IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Original) A semiconductor device assembly, comprising:
at least one semiconductor device; and
a plurality of mutually laterally spaced discrete spacers protruding from a surface of said at least one semiconductor device, said spacers defining a distance said surface of said at least one semiconductor device is to be spaced apart from another semiconductor device to be positioned in superimposed relation with said at least one semiconductor device.

2. (Original) The semiconductor device assembly of claim 1, wherein at least one of said spacers is resiliently compressible.

3. (Original) The semiconductor device assembly of claim 1, wherein at least one of said spacers protrudes from an active surface of said at least one semiconductor device.

4. (Previously presented) The semiconductor device assembly of claim 3, wherein each of said spacers protrudes from said active surface of said at least one semiconductor device.

5. (Original) The semiconductor device assembly of claim 4, wherein said plurality of spacers are arranged to stably support said another semiconductor device.

6. (Original) The semiconductor device assembly of claim 1, further comprising:
said another semiconductor device positioned adjacent said spacers, opposite from said at least one semiconductor device.

7. (Original) The semiconductor device assembly of claim 6, further comprising: adhesive material between said at least one semiconductor device and said another semiconductor device.

8. (Original) The semiconductor device assembly of claim 7, wherein said adhesive material is located between adjacent spacers.

9. (Original) The semiconductor device assembly of claim 6, wherein said spacers are electrically isolated from internal circuitry of said at least one semiconductor device.

10. (Original) The semiconductor device assembly of claim 1, wherein said spacers comprise electrically conductive material.

11. (Original) The semiconductor device assembly of claim 10, wherein said spacers communicate with a ground plane of said at least one semiconductor device.

12. (Original) The semiconductor device assembly of claim 1, further comprising: a substrate with which at least one semiconductor device is associated.

13. (Original) The semiconductor device assembly of claim 12, wherein said substrate comprises at least one of a circuit board, an interposer, a semiconductor device, and leads.

14. (Original) The semiconductor device assembly of claim 12, wherein at least one bond pad of said at least one semiconductor device is in communication with a corresponding contact area of said substrate.

15. (Original) The semiconductor device assembly of claim 14, further comprising:
at least one discrete conductive element extending from said at least one bond pad, over an active surface of said at least one semiconductor device, to said corresponding contact area.

16. (Previously presented) The semiconductor device assembly of claim 15, wherein heights of said spacers exceed a maximum height said at least one discrete conductive element protrudes above said active surface.

17. (Original) The semiconductor device assembly of claim 1, wherein said spacers are secured to noncircuit bond pads of said at least one semiconductor device.

18. (Original) A semiconductor device assembly, comprising:
a substrate;
a first semiconductor device associated with said substrate, bond pads of said first semiconductor device in communication with corresponding contact areas of said substrate;
mutually laterally spaced discrete spacers positioned on and protruding from an active surface of said first semiconductor device; and
a second semiconductor device comprising a back side positioned on said mutually laterally spaced discrete spacers.

19. (Original) The semiconductor device assembly of claim 18, wherein said substrate comprises one of a circuit board, an interposer, another semiconductor device, and leads.

20. (Currently amended) The semiconductor device assembly of claim 18, wherein said bond pads and said corresponding contact areas communicate ~~comminicate~~ by way of discrete conductive elements positioned therebetween.

21. (Original) The semiconductor device assembly of claim 20, wherein said discrete conductive elements comprise at least one of bond wires, tape-automated bond elements, and thermocompression bonded leads.

22. (Original) The semiconductor device of claim 18, wherein said mutually laterally spaced discrete spacers are secured to noncircuit bond pads of said first semiconductor device.

23. (Previously presented) The semiconductor device assembly of claim 22, wherein said mutually laterally spaced discrete spacers comprise conductive material.

24. (Original) The semiconductor device assembly of claim 23, wherein said mutually laterally spaced discrete spacers are electrically isolated from internal circuitry of said first semiconductor device.

25. (Original) The semiconductor device assembly of claim 23, wherein said mutually laterally spaced discrete spacers are in communication with a ground or reference voltage plane of said first semiconductor device.

26. (Original) The semiconductor device assembly of claim 25, wherein said back side of said second semiconductor device is also in communication with said ground or reference voltage plane.

27. (Previously presented) The semiconductor device assembly of claim 20, wherein heights of said mutually laterally spaced discrete spacers exceed a maximum height said discrete conductive elements protrude above said active surface.

28. (Previously presented) The semiconductor device assembly of claim 18, wherein at least one of said mutually laterally spaced discrete spacers is compressible.

29. (Previously presented) The semiconductor device assembly of claim 18, wherein said second semiconductor device comprises a dielectric layer on at least portions thereof that contact said mutually laterally spaced discrete spacers.

30. (Previously presented) The semiconductor device assembly of claim 18, wherein bond pads of said second semiconductor device communicate with said corresponding contact areas of said substrate by way of discrete conductive elements positioned therebetween.

31. (Original) The semiconductor device assembly of claim 18, further comprising: an adhesive layer between said first semiconductor device and said second semiconductor device.

32. (Original) The semiconductor device assembly of claim 31, wherein at least some of said mutually laterally spaced discrete spacers extend through said adhesive layer.

33. (Original) The semiconductor device assembly of claim 18, further comprising: at least one additional semiconductor device positioned over said second semiconductor device.

34. (Previously presented) The semiconductor device assembly of claim 18, further comprising:

an encapsulant material substantially covering said first semiconductor device, said second semiconductor device, discrete conductive elements, and portions of said substrate located adjacent to said first semiconductor device.

35. (Original) The semiconductor device assembly of claim 18, further comprising: at least one external connective element carried by said substrate and in electrical communication with at least one corresponding contact area of said substrate.

36-52. (Canceled)